EE105 – Fall 2014
Microelectronic Devices and Circuits

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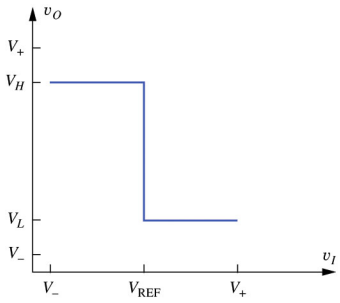
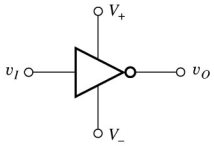
The Ideal Inverter

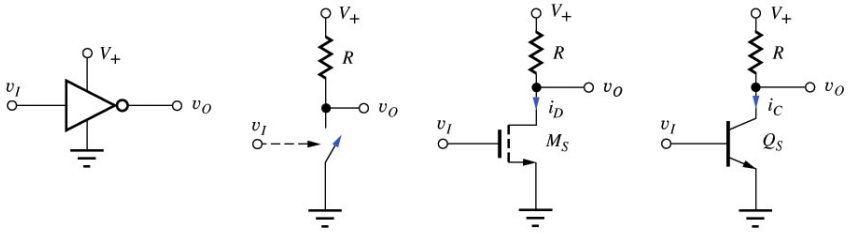
The ideal inverter has the following voltage transfer characteristic (VTC) and is described by the following symbol





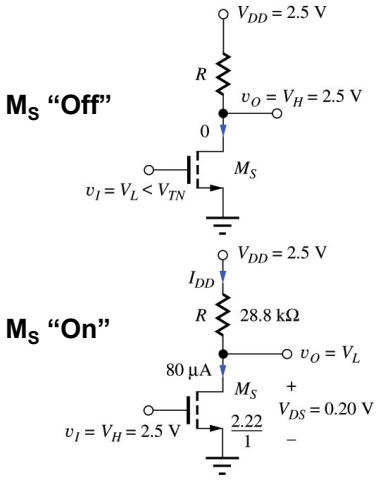
V_+ and V_- are the supply rails, and V_H and V_L describe the high and low logic levels at the output

Logic Level Definitions



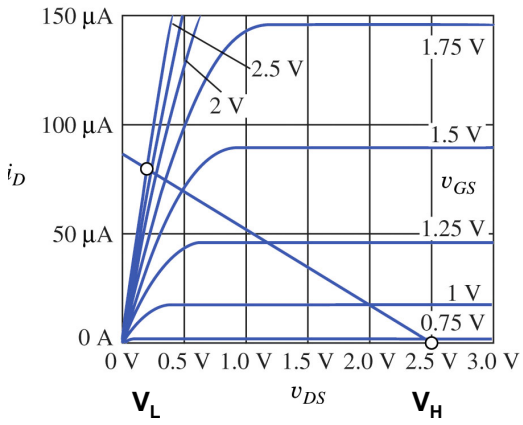
- An inverter operating with power supplies at V_+ and 0 V can be implemented using a switch with a resistive load
- The switch could be a mechanical device such as a wall switch or relay, a vacuum tube, or an MOS or bipolar transistor

NMOS Inverter with a Resistive Load



- Resistor R is used to "pull" the output high.
- MS is the switching transistor used to force the output low.
- The size of R and the W/L ratio of M_S are the design factors that need to be chosen.

NMOS Inverter with a Resistive Load
Load Line Visualization

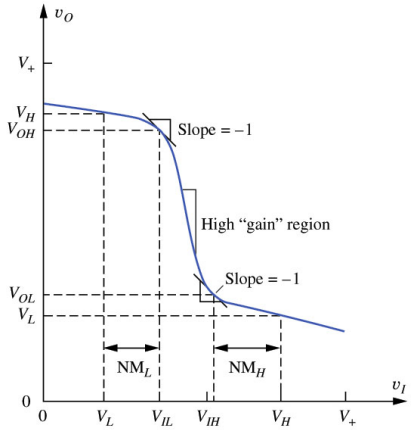


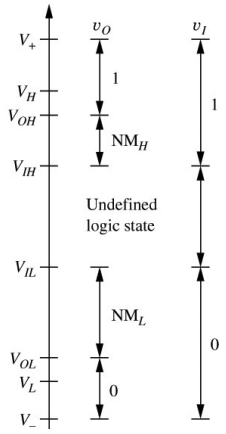
Q-pts for V_L and V_H on the NMOS device output (i_D -v_{DS}) characteristics.

Load line equation:

$$v_{DS} = V_{DD} - i_D R$$

Logic Level Definitions
Voltage Levels (cont.)





Note that for the voltage transfer characteristic (VTC) of the nonideal inverter, there is now an undefined logic state.

Noise Margin:
$NM_H = V_{OH} – V_{IH}$
$NM_L = V_{IL} - V_{OL}$

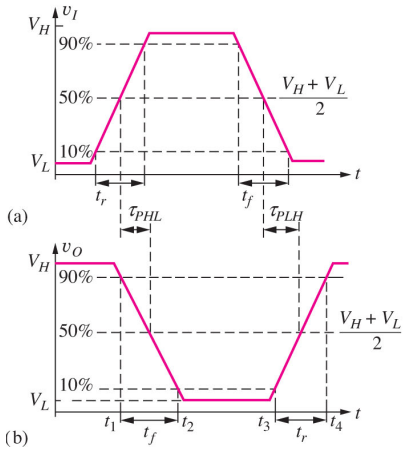
Logic Level Definitions
Voltage Levels

- V_L – The nominal voltage corresponding to a low-logic state at the output of a logic gate for $v_i = V_H$
- V_H – The nominal voltage corresponding to a high-logic state at the output of a logic gate for $v_i = V_L$
- V_{IL} – The maximum input voltage that will be recognized as a low input logic level
- V_{IH} – The maximum input voltage that will be recognized as a high input logic level
- V_{OH} – The output voltage corresponding to an input voltage of V_{IL}
- V_{OL} – The output voltage corresponding to an input voltage of V_{IH}

Logic Gate Design Goals

- An ideal logic gate is highly nonlinear and attempts to quantize the input signal to two discrete states. In an actual gate, the designer should attempt to minimize the undefined input region while maximizing noise margins.
- The input should produce a well-defined output, and changes at the output should have no effect on the input.
- Voltage levels at the output of one gate should be compatible with the input levels of a following gate.
- The gate should have sufficient fan-out and fan-in capabilities.
- The gate should consume minimal power (and area for ICs) and still operate under the design specifications.

Dynamic Response of Logic Gates
Propagation Delay



- **Propagation delay describes the amount of time between the input reaching the 50% point and the output reaching the 50% point.**

$$V_{50\%} = \frac{V_H + V_L}{2}$$

- **The high-to-low propagation delay, τ_{PHL}, and the low-to-high propagation delay, τ_{PLH}, are usually not equal, but can be combined as an average value:**

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

Dynamic Response of Logic Gates
Power-Delay Product

- **The power-delay product (PDP) is a metric that describes the amount of energy (Joules) required to perform a basic logic operation and is given by the following equation where P is the average power dissipated by the logic gate:**

$$PDP = P\tau_P$$

Review of Boolean Algebra

A	Z
0	1
1	0

NOT Truth Table

$Z = \overline{A}$

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

OR Truth Table

$Z = A + B$

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND Truth Table

$Z = AB$

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

NOR Truth Table

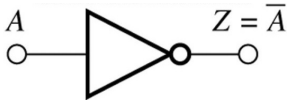
$Z = \overline{A + B}$

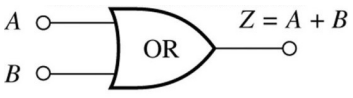
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

NAND Truth Table

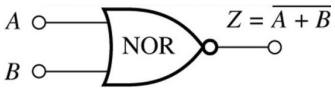
$Z = \overline{AB}$

Logic Gate Symbols and Boolean Expressions





(a)

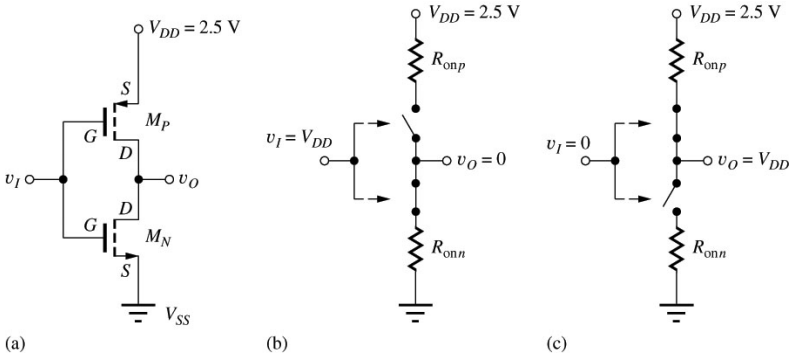


(a)

CMOS Technology

- Complementary MOS, or CMOS, needs both PMOS and NMOS devices for the logic gates to be realized
- The concept of CMOS was introduced in 1963 by Wanlass and Sah, but it did not become common until the 1980's as NMOS microprocessors were dissipating as much as 50 W and an alternative design technique was needed
- CMOS dominates digital IC design today

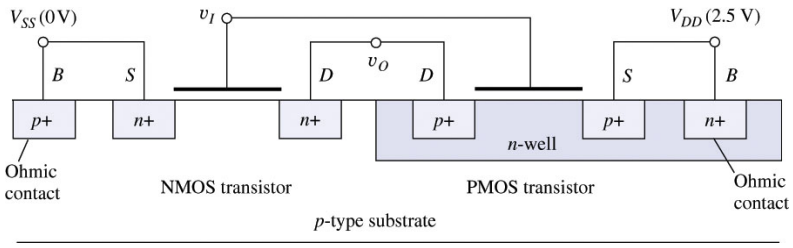
CMOS Inverter Circuit



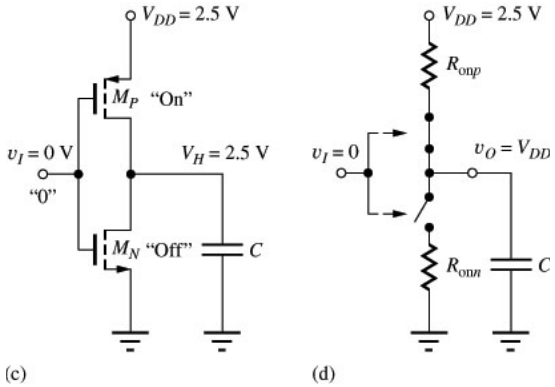
- When v_I is pulled high (to V_{DD}), the PMOS transistor is turned off, while the NMOS device is turned on pulling the output down to V_{SS}
- When v_I is pulled low (to V_{SS}), the NMOS transistor is turned off, while the PMOS device is turned on pulling the output up to V_{DD}

CMOS Inverter Fabrication

- The CMOS inverter consists of a PMOS device stacked on top on an NMOS device, but they need to be fabricated on the same wafer
- To accomplish this, the technique of "n-well" implantation was developed as shown in this cross-section of a CMOS inverter

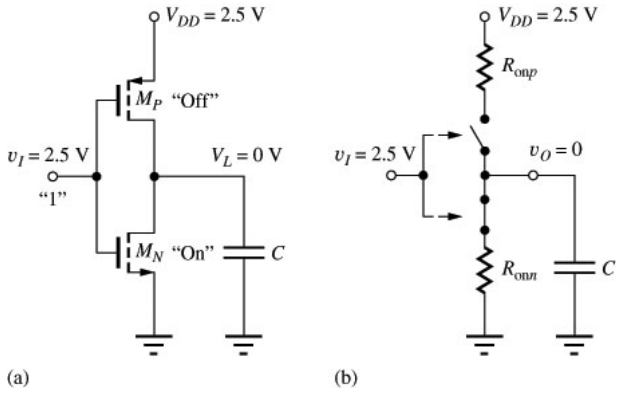


CMOS Inverter Static Characteristics: $v_I = V_L$



- For $v_I = V_L \leq V_{TN}$, M_N is off, and M_P is on. Therefore $V_H = V_{DD}$, $I_D = 0$, and there is no static power dissipation.

CMOS Inverter
Static Characteristics: $v_I = V_H$

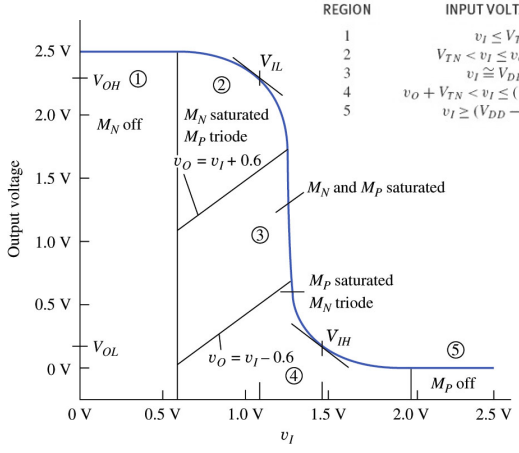


- For $v_I = V_H = V_{DD}$, $V_L = 0$ V, and $I_D = 0$ A which means that there is no static power dissipation

CMOS Inverter
Voltage Transfer Characteristics

Regions of Operation of Transistors in a Symmetrical CMOS Inverter

REGION	INPUT VOLTAGE v_I	OUTPUT VOLTAGE v_O	NMOS TRANSISTOR	PMOS TRANSISTOR
1	$v_I \le V_{TN}$	$V_H = V_{DD}$	Cutoff	Triode
2	$V_{TN} < v_I \le v_O + V_{TP}$	High	Saturation	Triode
3	$v_I \cong V_{DD}/2$	$V_{DD}/2$	Saturation	Saturation
4	$v_O + V_{TN} < v_I \le (V_{DD} - \lvert V_{TP}\rvert)$	Low	Triode	Saturation
5	$v_I \ge (V_{DD} - \lvert V_{TP}\rvert)$	$V_L = 0$	Triode	Cutoff



The VTC shown is for a CMOS inverter that is symmetrical ($K_p = K_n$).

CMOS Inverter
Noise Margins (cont.)

$$K_R = \frac{K_N}{K_P} \qquad NM_L = V_{IL} - V_{OL} \qquad NM_H = V_{OH} - V_{IH}$$

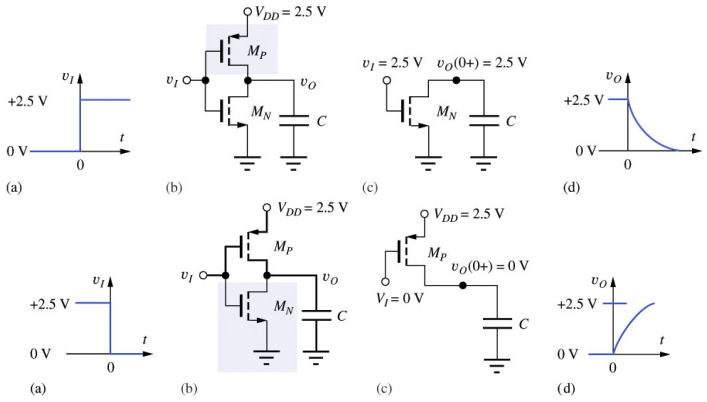
$$V_{IH} = \frac{2K_R\left(V_{DD} - V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)\sqrt{1 + 3K_R}} - \frac{\left(V_{DD} - K_R V_{TN} + V_{TP}\right)}{K_R - 1}$$

$$V_{OL} = \frac{\left(K_R + 1\right)V_{IH} - V_{DD} - K_R V_{TN} - V_{TP}}{2K_R}$$

$$V_{IL} = \frac{2\sqrt{K_R}\left(V_{DD} - V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)\sqrt{K_R + 3}} - \frac{\left(V_{DD} - K_R V_{TN} + V_{TP}\right)}{K_R - 1}$$

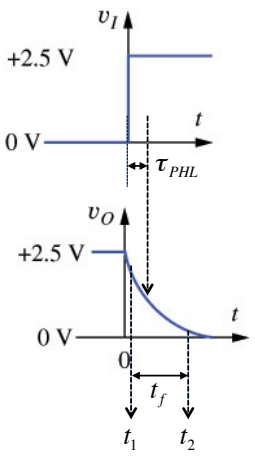
$$V_{OH} = \frac{\left(K_R + 1\right)V_{IL} + V_{DD} - K_R V_{TN} - V_{TP}}{2}$$

CMOS Inverter
Propagation Delay Estimate



- **The two modes of capacitive charging/discharging that contribute to propagation delay**

CMOS Inverter
Rise and Fall Times



RC charging (or discharging) is exponential:

$$\Delta v(t) = \Delta V \exp\left(-\frac{t}{RC}\right)$$

$$\text{At } 10\%,\ 0.1 = \exp\left(-\frac{t_1}{RC}\right)$$

$$\text{At } 90\%,\ 0.9 = \exp\left(-\frac{t_2}{RC}\right)$$

$$\text{Fall time: } t_f = t_2 - t_1 = RC\ln\left(\frac{0.9}{0.1}\right) = 2.2RC$$

$$\text{At } 50\%,\ 0.5 = \exp\left(-\frac{\tau_{PHL}}{RC}\right) \Rightarrow \tau_{PHL} = 0.69RC$$

Therefore, $t_f \cong 3\tau_{PHL}$

Similarly, $t_r \cong 3\tau_{PLH}$

CMOS Inverter
Propagation Delay Estimate (cont.)

$$\tau_{PHL} = R_{onN}C\left\{\ln\left[4\left(\frac{V_H - V_{TN}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TN}}{V_H - V_{TN}}\right\}$$

$$R_{onN} = \frac{1}{K_n\left(V_H - V_{TN}\right)}$$

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \tau_{PHL} = 1.2R_{onN}C$$

- **If it is assumed the inverter in "symmetrical" with $(W/L)_P = 2.5(W/L)_N$, then $\tau_{PLH} = \tau_{PHL}$**

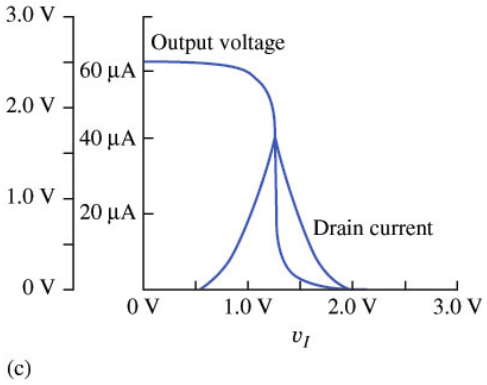
CMOS Inverter
Performance Scaling

- **State-of-the-art short gate length technologies are hard to analyze**
- **Scaling can be used to properly set W/L for a given load capacitance relative to reference gate simulation with a reference load.**

$$\tau_P = \frac{(W/L)}{(W/L)'} \times \left(\frac{C_L'}{C_{Lref}}\right) \times \tau_{Pref} \quad \text{or} \quad \left(\frac{W}{L}\right)' = \left(\frac{W}{L}\right) \times \left(\frac{\tau_{Pref}}{\tau_P}\right) \times \left(\frac{C_L'}{C_{Lref}}\right)$$

- **Scaling allows us to calculate a new geometry (W/L)' in terms of a target load and delay.**

CMOS Logic
Dynamic Power Dissipation



(c)

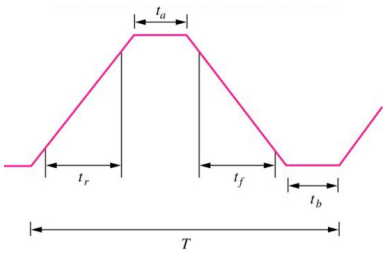
- **There are two components that add to dynamic power dissipation:**
  - **Capacitive load charging at a frequency f given by: PD = $CV_{DD}^2 f$**
  - **The current that occurs during switching which can be seen in the figure**

CMOS Logic
Power-Delay Product

- **The power-delay product is given as:**

$$PDP = P_{av}\tau_P$$

$$P_{av} = CV_{DD}^2 f = CV_{DD}^2 \frac{1}{T}$$



- **The figure shows a symmetrical inverter switching waveform**

$$T \geq t_r + t_a + t_f + t_b = \frac{2t_r}{0.8} = \frac{2(2\tau_P)}{0.8} = 5\tau_P$$

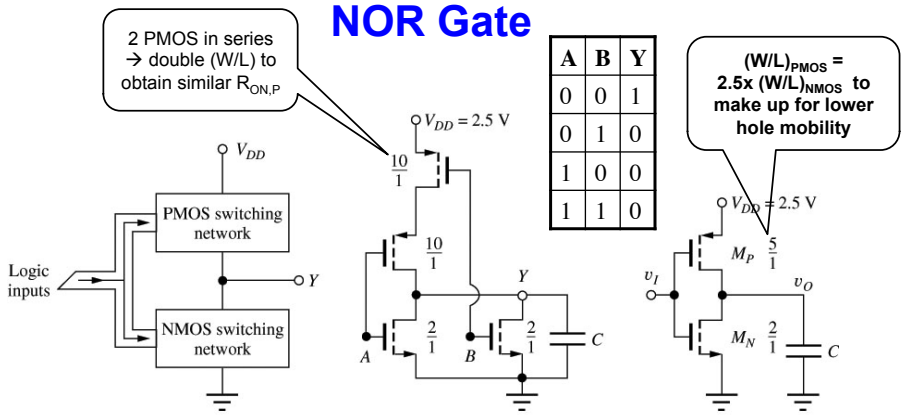
$$PDP \geq \frac{CV_{DD}^2}{5\tau_P}\tau_P = \frac{CV_{DD}^2}{5}$$

CMOS Logic
NOR Gate

2 PMOS in series → double (W/L) to obtain similar $R_{ON,P}$

$(W/L)_{PMOS}$ = 2.5x $(W/L)_{NMOS}$ to make up for lower hole mobility

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

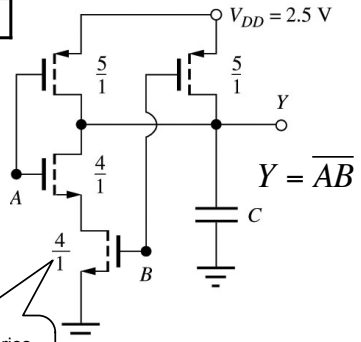


$$Y = \overline{A + B}$$

Basic CMOS logic gate structure | **CMOS NOR gate implementation** | **Reference Inverter**

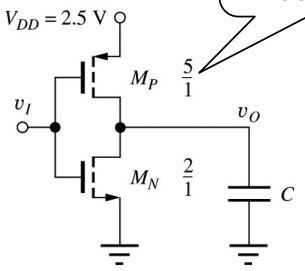
CMOS Logic NAND Gates

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



2 NMOS in series → double (W/L) to obtain similar $R_{ON,N}$

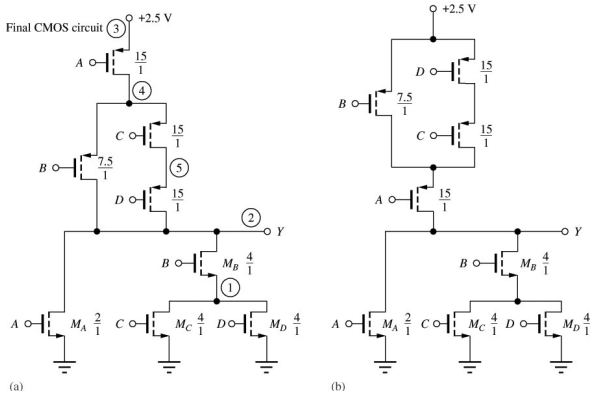
CMOS NAND gate implementation



Reference Inverter

$(W/L)_{PMOS}$ is usually 2.5x $(W/L)_{NMOS}$ to make up for lower hole mobility

Complex CMOS Logic Gate Design Example (cont.)



Two equivalent forms of the final circuit

- **From the PMOS graph, the PMOS network can now be drawn for the final CMOS logic gate while once again considering the longest PMOS path for sizing**